REMARKS

The specification has been amended to correct portions pointed out by the Examiner.

Proposed changes to the drawings are indicated in red. Approval is hereby requested.

Before discussing the claims and how they distinguish over the cited art, perhaps it might be helpful to review features of applicant's invention.

Referring to FIG, 2 of the patent application, the system 100 includes a plurality of front end directors 180_1-180_{32} and back end directors 200_1-200_{32}. These directors are connected to: (1) a data transfer section 240, and more particularly to a global cache memory 220 of such data transfer section); and, (2) a message network 260. The message network 260 operates independently of the data transfer section 240.

Referring now to the claims, the claims point out that system interface includes BOTH a data transfer section AND a message network.

Referring now to the rejection, the examiner refers to the data section as memory regions A-D in Fig. 3 of Walton and the message network as cache memory 120_0 and 120_1 in Fig. 2 of Walton. ***However, these are the same.*** Referring to Fig. 3 of Walton, the memory regions A-D and the coupling node ***are part of the memory board 120_0***. Thus, the cache memory of Walton appears to be considered by the Examiner as both the data transfer section and the message network. The claims however point out: (1) that the a message network operates independently of the data transfer section; and (2) that the message network comprises a switching network having a plurality input/output ports, each one of such pair of input/output ports being coupled to a corresponding one of the pair of output/input ports of the crossbar switches of the plurality of first director boards and the plurality of second director boards. Thus, if the switch on the memory board of Walton is considered by the Examiner as the message network it is not understood how this network, as defined by the Examiner, operates independently of the data transfer section, i.e., the cache memory.

With regard to Gilbertson et al., U. S. Patent No. 6,178,466, such patent does not describe a message network comprising a switching network having a plurality input/output ports, each

one of such pair of input/output ports being coupled to a corresponding one of the pair of output/input ports of the crossbar switches of the plurality of first director boards and the plurality of second director boards. There is nothing in Gilberston et al. which describes or suggests that the message network operate independently of the data transfer section where the message network comprises a switching network having a plurality input/output ports, each one of such pair of input/output ports being coupled to a corresponding one of the pair of output/input ports of the crossbar switches of the plurality of first director boards and the plurality of second director boards.

In the event any additional fee is required, please charge such amount to Patent and Trademark Office Deposit Account No. 50-0845.

Respectfully submitted,

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Attachment: Sheets of Specification with Markings showing changes made
EMC2-43PUS-response to office action dated 10_03_02.doc

COMPARISON SPECIFICATION

Paragraph beginning on page 10, line 18

Referring now to FIGS. 3 and 4, the system interface 160 is shown to include an electrical cabinet 300 having stored therein: a plurality of, here eight front-end director boards 190_1-190_8, only board 190_1 being shown in FIG. 4, each one having here four of the front-end directors 180_1-180_{32}; a plurality of, here eight back-end director boards 210_1-210_8, only board 210_8 being shown in FIG. 4, each one having here four of the back-end directors 200_1-200_{32}; and a plurality of, here eight, memory boards 220' which together make up the global cache memory 220. These boards plug into the front side of a backplane 302. (It is noted that the backplane 302 is a mid-plane printed circuit board). Plugged into the backside of the backplane 302 are message network boards 304_1, 304_2. The backside of the backplane 302 has plugged into it adapter boards, not shown in FIGS. 2-4, which couple the boards plugged into the back-side of the backplane 302 with the computer 120 and the bank of disk drives 140 as shown in FIG. 2. That is, referring again briefly to FIG. 2, an I/O adapter, not shown, is coupled between each one of the front-end directors 180_1-180_{32} and the host computer 120 and an I/O adapter, not shown, is coupled between each one of the back-end directors 200_1-200_{32} and the bank of disk drives 140.

Paragraph beginning on page 6, line 17:

Referring now to FIG. 2, a data storage system 100 is shown for transferring data between a host computer/server 120 and a bank of disk drives 140 through a system interface 160. The system interface 160 includes: a plurality of, here 32 front-end directors 180_1-180_{32} coupled to the host computer/server 120 via ports 123_1-123_{32}; a plurality of back-end directors 200_1-200_{32} coupled to the bank of disk drives 140 via ports 123_{33}-123_{64}; a data transfer section 240, having a global cache memory 220, coupled to the plurality of front-end directors 180_1-180_{16} and the back-end directors 200_1-200_{16}; and a messaging network 260, operative independently of the data transfer section 240, coupled to the plurality of front-end directors 180_1-180_{32} and the plurality of back-end directors 200_1-200_{32}, as shown. The front-end and back-end directors 180_1-180_{32}, 200_1-200_{32} are functionally similar and include a microprocessor (μP) 299 (i.e., a central processing unit (CPU) and RAM), a message engine/ CPU controller 314 and a data pipe 316 to be described in detail in connection with FIGS. 5, 6 and 7. Suffice it to say here, however, that the front-end and back-end directors 180_1-180_{32}, 200_1-200_{32} control data transfer between the host computer/server 120 and the bank of disk drives 140 in response to messages passing between the directors 180_1-180_{32}, 200_1-200_{32} through the messaging network 260. The messages facilitate the data transfer between host computer/server 120 and the bank of disk drives 140 with such data passing through the global cache memory 220 via the data transfer section 240. More particularly, in the case of the front-end directors 180_1-180_{32}, the data passes between the host computer to the global cache memory 220 through the data pipe 316 in the front-end directors 180_1-180_{32} and the messages pass through the message engine/CPU controller 314 in such front-end directors 180_1-180_{32}. In the case of the back-end directors 200_1-200_{32} the data passes between the back-end directors 200_1-200_{32} and the bank of disk drives 140 and the global cache memory 220 through the data pipe 316 in the back-end directors 200_1-200_{32} and again the messages pass through the message engine/CPU controller 314 in such back-end director 200_1-200_{32}.